APPROXIMATE RECURSIVE MULTIPLIERS USING LOW POWER BUILDING BLOCKS

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ABSTRACT

We are aware that during testing when the device's normal functioning mode is off, the dissipation of power is approximately 200% more than that of normal functioning mode. In this project 32-bit test pattern generator has been proposed for testing the VLSI design. This 32-bit test pattern generator is implemented with efficient LFSR and with extra combinational circuitry which achieved Low power consumption. The switching activity between the tests vector are reduced, this results in low power consumption.

INTRODUCTION

In modern integrated circuit (IC) design and development, ensuring the reliability, functionality, and performance of digital systems is a crucial task. With the increasing complexity of Very Large-Scale Integration (VLSI) circuits, testing has become a fundamental aspect of the design cycle to detect faults, ensure correctness, and improve yield. One of the essential components of digital testing is the generation of test patterns, which are used to stimulate the circuit under test (CUT) and observe its response to identify any defects. The efficiency of this process significantly impacts the overall performance, power consumption, and reliability of the testing environment.

Traditional methods of test pattern generation (TPG) often focus on maximizing fault coverage but tend to overlook key constraints such as power consumption, hardware overhead, and speed of operation. This is particularly critical for contemporary VLSI designs, where low power consumption and energy efficiency are paramount considerations due to the rise of portable and battery-operated devices, as well as the scaling down of technology nodes. Additionally, as IC complexity grows, the number of patterns required to test a circuit also increases, leading to greater power dissipation during testing, which can affect the lifespan of the device or even cause unintended functional behavior during testing.

This project, "Implementation of Efficient and Low Power Test Pattern Generators," addresses the challenges associated with traditional test pattern generation methods by proposing novel techniques that not only ensure high fault coverage but also emphasize efficiency in power consumption and resource utilization. The primary focus is to develop test pattern generators that are optimized for low power operation while maintaining or enhancing fault detection capabilities. By implementing these efficient TPGs, we aim to minimize the dynamic power dissipation during testing, reduce switching activity, and maintain the integrity of the testing process without compromising on fault coverage.

LITERATURE SURVEY

Girard et al. (2000) – "Low-Power Testing: A Survey"

Girard et al. provided one of the earliest comprehensive surveys on low-power testing methodologies, outlining the sources of power consumption during test processes, particularly the excessive switching activity caused by traditional test pattern generators like LFSRs. Their work emphasized the need for reducing the power dissipated during testing, especially in larger circuits. However, the survey did not offer specific solutions for mitigating power consumption in TPGs, highlighting a gap for further research in this area.

Wang et al. (2001) – "Low-Transition Test Pattern Generation"

This study introduced Low-Transition Linear Feedback Shift Registers (LT-LFSRs), which reduced power consumption by minimizing switching activity during test pattern application. Wang et al.'s approach was a significant improvement over traditional LFSRs, reducing dynamic power by lowering the number of transitions between consecutive test vectors. Despite the effectiveness of LT-LFSRs in reducing power, the authors did not explore the impact on fault coverage in more complex fault models like bridging or transition faults, which limits the overall applicability in broader testing scenarios.

Chandra and Chakrabarty (2002) – "Test Data Compression and Test Power Reduction" Chandra and Chakrabarty's work focused on test data compression as a means of reducing power consumption during testing. By compressing test data, they reduced the number of bits that needed to be shifted into the scan chain, which in turn lowered the switching activity. However, the study primarily addressed the compression of deterministic test vectors rather than random test patterns, limiting its applicability to scenarios where random patterns are essential for fault coverage.

Wen et al. (2005) – "Power-Aware Test Pattern Generation for Scan-Based Testing"

Wen et al. presented a power-aware test pattern generation approach that reduced the switching activity in scan-based designs by carefully generating test patterns with fewer transitions. This method reduced power consumption during scan operations and improved reliability in circuits under test. However, the study focused primarily on reducing power during scan operations and did not extend its analysis to non-scan or combinational circuits, limiting the generalizability of the approach to different circuit types.

PROPOSED SYSTEM

This project focuses on low-power LT-LFSR based test pattern generator that can be used for testing of both combinatorial and sequential circuits. The proposed architecture step-up the correlation between the two tests vectors which reduces the number of transitions i.e. switching activities between two test vectors. Minimizing the switching activity between test vectors will result in reducing the power consumption. The conventional LFSR architecture is to be customized in such a way that it routinely injects intermediate patterns between its unique pair of patterns. This can be done by using two schemes i.e. Bipartite and random injection, which is further discussed in this section and with a minimal number of switching activity between two test vectors.

We propose a Low Transition Test Pattern Generator that introduces two techniques for test vectors generation called Random Injection (RI) and Bipartite LFSR. In brief, the RI technique injects a new pattern between two successive test patterns by using a random-bit injection (R) whether it can be either ‘0’ or ‘1’, in the consequent bit of an intermediate pattern where there is transition occurs in the corresponding bit of pattern pairs.

Low-Transition Pattern Generation Techniques

The Random injection method inserts a new test vector Ti1 between two test vector such that the summation of the switching activities between Ti and Ti1 and Ti1 and Ti+1 is same as the switching activity between the Ti

$$\sum_{j=1}^{n} |t_j^i - t_j^{i1}| + \sum_{j=1}^{n} |t_j^{i1} - t_j^{i+1}| = \sum_{j=1}^{n} |t_j^i - t_j^{i+1}| \quad \text{.....(1)}$$

and Ti+1.

Therefore, by inserting the Ti1 bit pattern in between Ti and Ti+1, which reduces the switching activities between Ti and Ti+1.Whenever two equal-bit position is same between Ti and Ti+1, then the same bit is injected in that position. When a transition occurs between the Ti and Ti+1 then the RI injection i

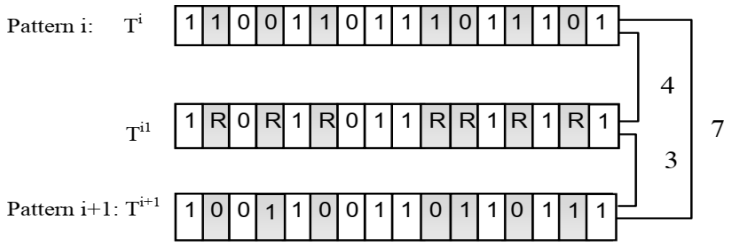
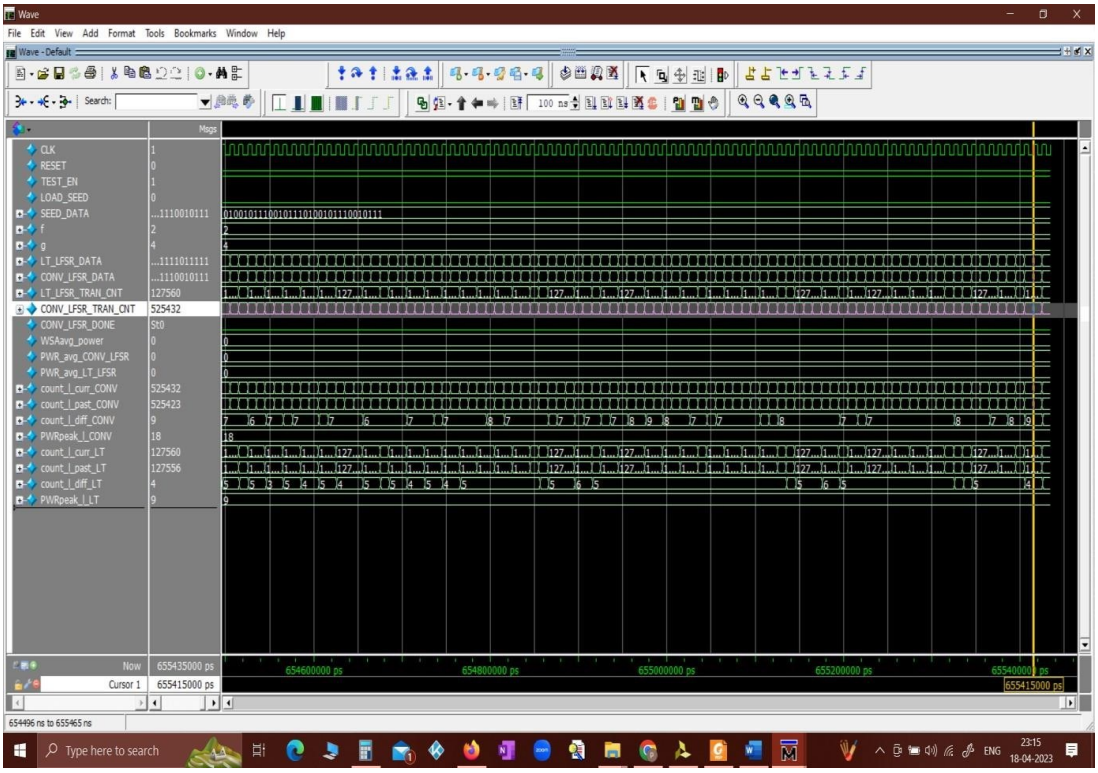


Fig. 2: Example of RI injection (R=0)

Figure.1 RI injection



SIMULATION RESULTS

Figure.2 Simulation output

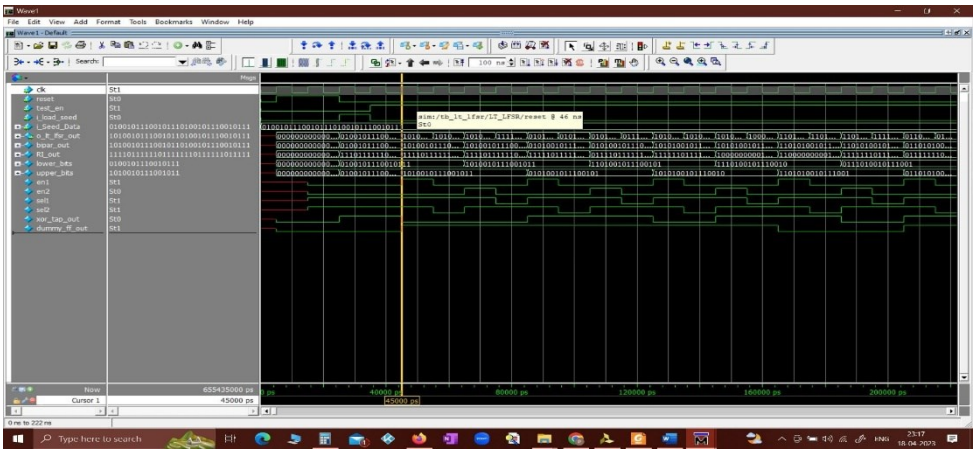


Figure.2 Simulation output2

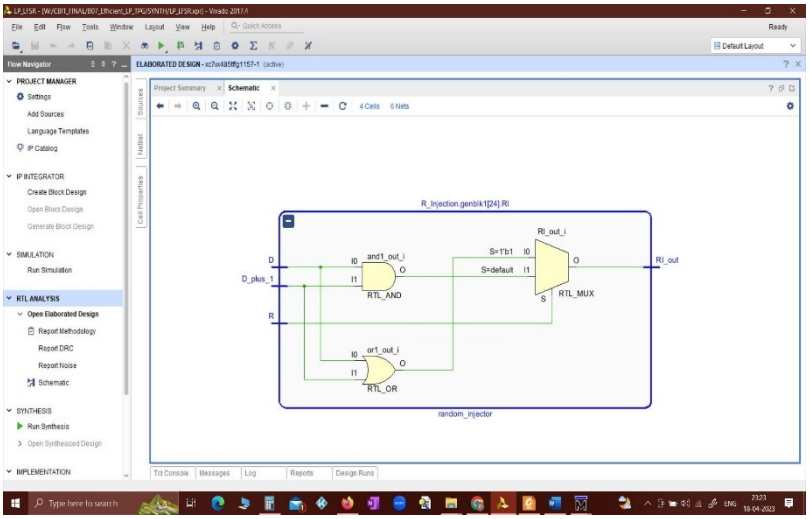


Figure.3 RTL Output1

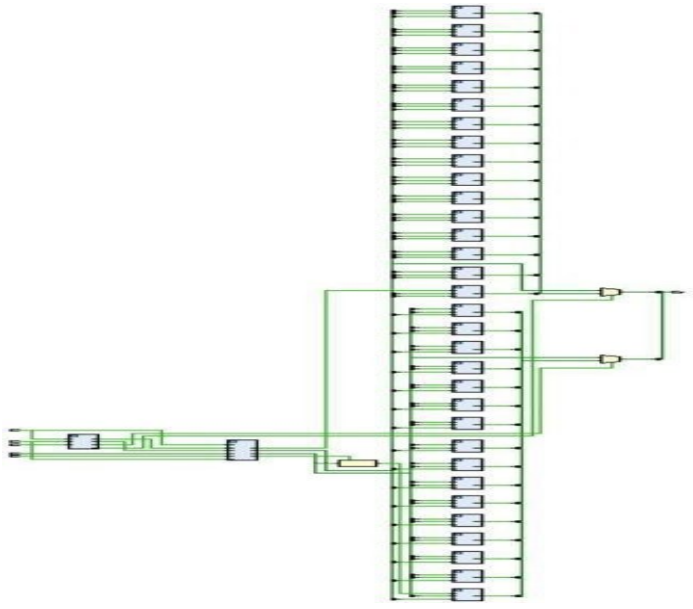


Figure.4 RIL Outpu2

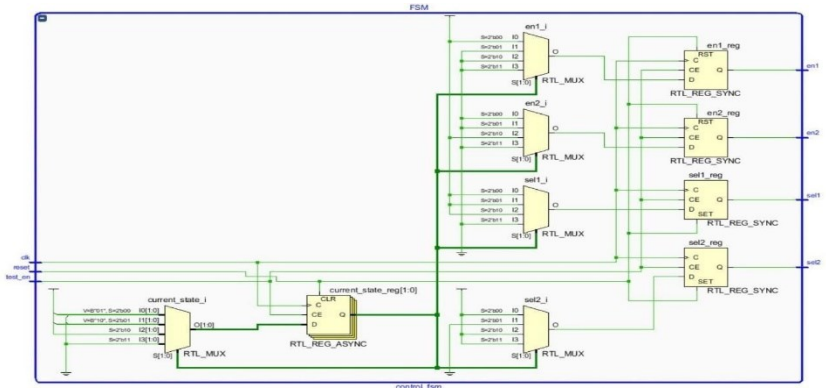


Figure.5 RTL Output3

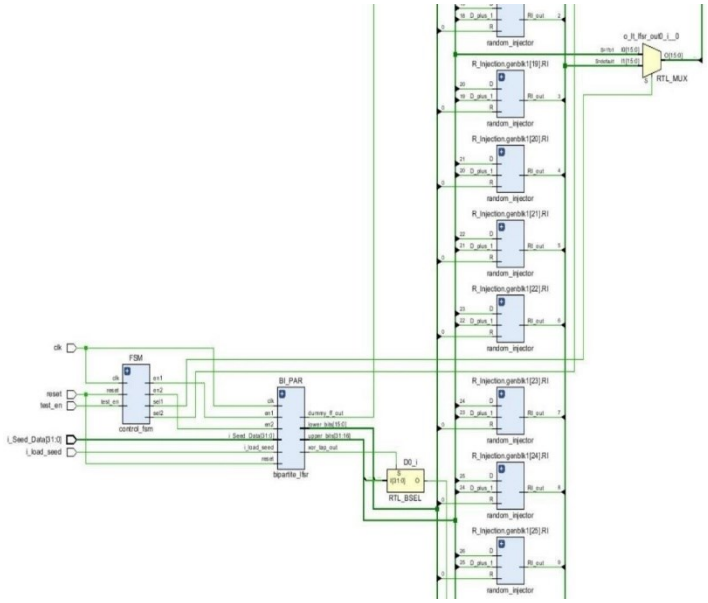


Figure.6 RTL Output

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	132	0	303600	0.04
LUT as Logic	132	0	303600	0.04
LUT as Memory	0	0	130800	0.00
Slice Registers	103	0	607200	0.02
Register as Flip Flop	71	0	607200	0.01
Register as Latch	32	0	607200	<0.01
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure.7 Area Report

Ref Name	Used	Functional Category
LUT3	96	LUT
IBUF	36	IO
FDCE	35	Flop & Latch
OBUF	32	IO
LUT6	32	LUT
LDCE	32	Flop & Latch
FDPE	32	Flop & Latch
LUT2	6	LUT
BUFG	3	Clock
FDSE	2	Flop & Latch
FDRE	2	Flop & Latch
LUT1	1	LUT

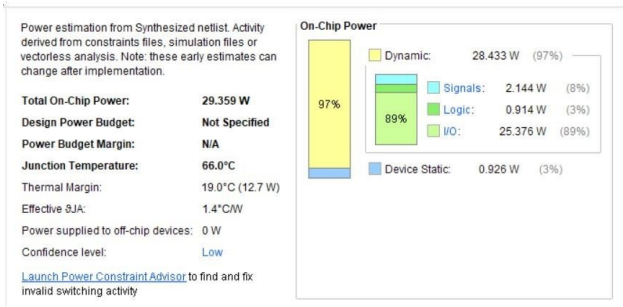


Figure.8 PRIMITIVES_USED_LP_LFSR

Figure.9 Power Report

ADVANTAGES

1. **Reduced power consumption:** LPTPGs are specifically designed to generate test patterns that consume less power compared to traditional test pattern generators. This means that LPTPGs are ideal for testing low-power circuits, such as those found in portable electronic devices.
2. **Faster testing:** LPTPGs can generate test patterns much faster than traditional test pattern generators, which means that they can speed up the testing process and reduce overall testing time.
3. **Improved accuracy:** LPTPGs can generate test patterns with greater accuracy, which means that they can help identify problems in circuits more effectively. This is particularly important in complex circuits where identifying problems can be challenging.
4. **Cost-effective:** LPTPGs can be less expensive than traditional test pattern generators, which means that they can be an affordable option for companies that need to test a large number of circuits.
5. **Easy to use:** LPTPGs are often designed to be user-friendly, with simple interfaces and easy-to-understand instructions. This means that they can be used by technicians with minimal training, which can save time and money in the testing process.

APPLICATIONS

1. **Mobile devices:** LPTPGs are ideal for testing the low-power circuits found in mobile devices, such as smartphones, tablets, and wearables. These devices require long battery life, and LPTPGs can generate test patterns that consume less power, which is important for preserving battery life.

2. **Internet of Things (IoT):** LPTPGs are also commonly used in the testing of IoT devices, which often have low-power requirements due to their limited power sources, such as batteries. LPTPGs can generate test patterns that are specifically designed for low-power IoT devices, which can help ensure that these devices function correctly and efficiently.
3. **Automotive electronics:** LPTPGs are used to test the electronic systems in automobiles, such as engine management systems and advanced driver assistance systems (ADAS). These systems have strict power requirements, and LPTPGs can help ensure that they operate correctly while minimizing power consumption.
4. **Aerospace and defence**: LPTPGs are used to test the electronic systems in aerospace and defence applications, such as aircraft control systems and missile guidance systems. These systems have strict power requirements and must operate reliably in harsh environments, making LPTPGs an essential tool for testing and verification.

CONCLUSION

This project shows an effective HDL implementation of low power utilization for test pattern generator usingtheLowPowerLFSRtechnique.Italsoaddressesatheorytoexpressatestpatterncreationbyusing LowTransitionLinearFeedbackShiftRegisterarchitecture.Byusingthistechnique;powerconsumption canbereducedascomparedtotheconventionalLFSRtechnique. Itshowsthatthetotalpower consumed inlowtransitionlinearfeedbackshiftregisteris50.06%lessthantheconventionalLFSR.Fromtheresults, it shows that LowPower LFSR is verymuchconstructive for power reductiontechniques during testing mode.

FUTURESCOPE

BIST(Built-InSelf-Test)isatechniqueusedinelectronichardwaredesigntotestintegratedcircuits(ICs) without requiring an externaltest equipment. BIST is becoming increasinglypopular because it offers a convenient and cost-effective way to test ICs during manufacturing and in-field testing.Lowpowertestpatterngenerators(LPTPGs)areanimportantcomponent ofBIST.LPTPGsgeneratetest patternsthat help detect faults inanIC'spower distributionnetwork,which iscrucialfor powerintegrity testing.

The future scope of LPTPGs in BIST is promising as low-power design techniques are becoming more prevalent inICs.WiththeincreasinguseofmobileandIoTdevices,low-powerconsumptionhasbecome acriticalfactorinICdesign.LPTPGscanhelpdetectpower-relatedfaultsinlow-powerICs,makingthem an essential tool for BIST.

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